CLAIMS

What is claimed is:

1. An architecture for transferring data from a first device to a second device, comprising:
   a) a clock recovery loop receiving said data from said first device, said clock recovery loop providing a recovered clock signal;
   b) a filter circuit configured to filter information from said recovered clock signal and provide a transmitter clock adjustment signal that adjusts said transmitter clock in response to inputs from (i) said clock recovery loop and (ii) a transmitter clock circuit; and
   c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal.

2. The architecture of claim 1, further comprising a receiver in communication with said clock recovery loop and said filter circuit, configured to receive said data from a network.

3. The architecture of claim 1, wherein said clock recovery loop comprises a first phase detector configured to determine a phase difference between said recovered clock signal and either a reference clock signal or said data.

4. The architecture of claim 3, wherein said clock recovery loop further comprises a recovered clock adjustment circuit configured to adjust said recovered clock signal in response to said phase difference.

5. The architecture of claim 4, wherein said recovered clock adjustment circuit provides a recovered clock adjustment signal in response to said phase difference.

6. The architecture of claim 5, wherein said input from said clock recovery loop comprises said recovered clock adjustment signal, and said filter circuit is further configured to filter said recovered clock adjustment signal.

7. The architecture of claim 6, wherein said filter circuit is further configured to provide said transmitter clock adjustment signal in response to said filtered recovered clock adjustment signal and said input from said transmitter clock circuit.

8. The architecture of claim 7, wherein said input from said transmitter clock circuit comprises said transmitter clock signal.

9. The architecture of claim 8, wherein said filter circuit provides said transmitter clock adjustment signal in further response to said recovered clock signal, said filter circuit being further configured to determine a phase difference between said transmitter clock signal and said recovered clock signal.

10. The architecture of claim 1, wherein said filter circuit comprises a jitter reduction circuit configured to reduce jitter in said input from said clock recovery loop and provide a filtered clock information signal in response thereto.

11. The architecture of claim 10, wherein said filter circuit further comprises a clock alignment block configured to (i) receive said recovered clock signal and said transmitter clock signal and (ii) provide a data transfer control signal in response thereto.

12. The architecture of claim 11, wherein said filter circuit further comprises a logic circuit configured to mathematically combine said data transfer control signal and said filtered clock information signal and provide said transmitter clock adjustment signal in response thereto.

13. The architecture of claim 1, wherein said transmitter is configured to transmit serial data.

14. A circuit for facilitating data transfer, comprising:
    a) a clock alignment block configured to (i) receive first and second periodic signals and (ii) provide a data transfer control signal in response thereto;
    b) a first filter circuit configured to receive first periodic signal information and provide a filtered clock information signal in response thereto; and
    c) a logic circuit configured to combine said data transfer control signal and said filtered clock information signal and provide an adjustment signal for said second periodic signal in response thereto.

15. The circuit of Claim 14, wherein said first and second periodic signals comprise a recovered clock signal and a transmitter clock signal.

16. The circuit of Claim 14, wherein said clock alignment block comprises a first phase detector configured to receive said first and second periodic signals.

17. The circuit of Claim 16, wherein said clock alignment block further comprises a second filter circuit configured to filter an output of said phase detector and provide said data transfer control signal.

18. The circuit of Claim 17, wherein said second filter circuit comprises a multiplier configured to multiply said output of said phase detector by a first coefficient.

19. The circuit of Claim 18, wherein said second filter circuit further comprises a first integrator configured to integrate an output of said multiplier and provide said data transfer control signal.

20. The circuit of Claim 14, wherein said first filter circuit comprises a frequency tracking loop.

21. The circuit of Claim 20, wherein said frequency tracking loop comprises a first adder configured to add said first periodic signal information and said filtered clock information signal.

22. The circuit of Claim 21, wherein said frequency tracking loop further comprises a second multiplier configured to multiply an output of said first adder by a second coefficient.

23. The circuit of Claim 22, wherein said frequency tracking loop further comprises a second integrator configured to provide said filtered clock information signal.

24. The circuit of Claim 21, wherein said first filter circuit further comprises a phase adjustment circuit configured to receive said output of said first adder and provide a phase adjustment signal in response thereto.

25. The circuit of Claim 24, wherein said phase adjustment circuit comprises (i) a third multiplier configured to multiply an output of said first adder by a third coefficient, and (ii) a third integrator configured to provide said phase adjustment signal.

26. The circuit of Claim 14, wherein said logic circuit comprises a second adder.

27. A system, comprising:

a) the architecture of Claim 1; and

b) a receiver communicatively coupled to said clock recovery loop, configured to receive said data from a network and transfer said data to said transmitter.

28. The system of Claim 27, further comprising an oscillator configured to provide a reference clock signal to said transmitter and said receiver.

29. The system of Claim 27, embodied on a single integrated circuit.

30. The system of Claim 27, wherein said receiver is further configured to convert serial data from a network to parallel data for the transmitter.

31. The system of Claim 30, wherein said receiver further comprises a deserializer operating in accordance with the recovered clock signal.

32. The system of Claim 30, wherein said transmitter is further configured to convert parallel data from the receiver to serial data for transmission to a destination device.

33. The system of Claim 32, wherein said transmitter further comprises a serializer operating in accordance with the transmitter clock signal.

34. The system of Claim 27, further comprising a first port communicatively coupled to said receiver and a second port communicatively coupled to said transmitter, each of said first and second ports being configured to communicate with one or more external devices.

35. A multiport device, comprising:

a) a plurality of receivers, each coupled to a unique one of a plurality of clock recovery loops,

b) a plurality of transmitters, each coupled to a unique one of a plurality of filter circuits receiving recovered clock information from a corresponding one of the plurality of clock recovery loops, and

c) a plurality of data paths for transferring data from one of the plurality of receivers to one of the plurality of transmitters.

36. The multiport device of claim 35, further comprising a plurality of input ports communicatively coupled to the plurality of receivers, and a plurality of output ports communicatively coupled to the plurality of transmitters.

37. The multiport device of claim 35, further comprising a plurality of data path switches.

38. The multiport device of claim 37, wherein each of said data path switches communicatively couple an input port to at least a subset of the plurality of receivers in the multiport device.

39. The multiport device of claim 37, wherein each of said data path switches communicatively couple an output port to at least a subset of the plurality of transmitters in the multiport device.

40. The multiport device of claim 37, wherein each of said data path switches communicatively couple at least a subset of the plurality of receivers to at least a subset of the plurality of transmitters in the multiport device.

41. The multiport device of claim 35, embodied on a single integrated circuit.

42. A network, comprising:

a) a plurality of the systems of claim 27; and

b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to at least one of said systems.

43. The network of Claim 42, wherein said plurality of said systems are embodied on a single integrated circuit.

44. The network of Claim 42, wherein said plurality of said systems receives serial data from said plurality of storage or communications devices.

45. The network of claim 42, wherein a first one of said plurality of storage or communications devices operates at a first frequency, a second one of said plurality of storage or communications devices operates at a second frequency the same as or different from the first frequency, and said plurality of said systems operates at a third frequency the same as or different from either or both of the first and/or second frequencies.

46. The network of Claim 45, wherein each of said first and second devices and each of said plurality of said systems transmits serial data at a rate of at least 1 Gb/second.

47. The network of Claim 45, wherein each of said plurality of said systems transmits serial data at a rate F_3 that is about the same as at least one of a rate F_1 at which said first device transmits serial data and a rate F_2 at which said second device transmits serial data.

48. The network of Claim 42, further comprising a network controller or logic configured to select a first device of said plurality of storage or communications devices from which serial data is to be transmitted.

49. The network of Claim 48, wherein said network controller or logic is further configured to select a second device of said plurality of storage or communications devices to which serial data is to be transmitted.

50. The network of Claim 49, wherein said network controller or logic is further configured to select a data path through said plurality of said systems to receive said serial data from said first device and transmit said serial data to said second device.

51. An architecture for transferring data, comprising:
    a) means for recovering a clock signal from said data;
    b) means for filtering recovered clock signal information;
    c) means for adjusting a transmitter clock in response to (i) said filtered recovered clock signal information, (ii) said recovered clock signal and (iii) a transmitter clock signal; and
    d) means for transmitting said data to an external device in accordance with said transmitter clock signal.

52. The architecture of claim 51, further comprising a means for receiving said data.

53. The architecture of claim 51, wherein said means for recovering comprises a means for determining a phase difference between said recovered clock signal and either a reference clock signal or said data.

54. The architecture of claim 53, wherein said means for recovering further comprises a means for adjusting said recovered clock signal in response to said phase difference.

55. The architecture of claim 54, wherein said means for filtering filters an output of said means for adjusting said recovered clock signal.

56. The architecture of claim 51, wherein said means for filtering is configured to reduce jitter in said recovered clock signal information.

57. The architecture of claim 51, wherein said means for adjusting a transmitter clock further comprises a means for determining said difference between said recovered clock signal and said transmitter clock signal.

58. The architecture of claim 51, wherein said data comprises serial data.

59. A circuit, comprising:

a) means for detecting a difference between first and second periodic signals;

b) first means for filtering first periodic signal information; and

c) first means for combining an output of said means for detecting and an output of said first means for filtering, providing a control signal configured to reduce said difference between first and second periodic signals.

60. The circuit of Claim 59, wherein said first and second periodic signals comprise a recovered clock signal and a transmitter clock signal.

61. The circuit of Claim 59, wherein said means for detecting comprises (i) a first phase detector configured to receive said first and second periodic signals, and (ii) a second means for filtering an output of said phase detector.

62. The circuit of Claim 61, wherein said second means for filtering comprises a multiplier configured to multiply said output of said phase detector by a first coefficient.

63. The circuit of Claim 62, wherein said second means for filtering further comprises a first means for integrating an output of said multiplier.

64. The circuit of Claim 59, wherein said first means for filtering comprises a means for tracking a frequency of said first periodic signal.

65. The circuit of Claim 64, wherein said means for tracking comprises a second means for combining said first periodic signal information and said filtered periodic signal information.

66. The circuit of Claim 65, wherein said means for tracking further comprises a second means for multiplying an output of said second means for combining by a second coefficient.

67. The circuit of Claim 66, wherein said means for tracking further comprises a second means for integrating configured to provide said filtered clock information signal.

68. The circuit of Claim 65, wherein said first means for filtering further comprises a third means for filtering an output of said second means for combining.

69. The circuit of Claim 68, wherein said third means for filtering comprises (i) a third means for multiplying said output of said second means for combining by a third coefficient, and (ii) a third means for integrating an output of said third means for multiplying.

70. The circuit of Claim 59, wherein said first means for combining comprises a means for adding said output of said means for detecting and said output of said first means for filtering.

71. A system, comprising:

a) the architecture of claim 51; and

b) a means for receiving said data, communicatively coupled to said means for recovering said clock signal, configured to receive said data from a network and transfer said data to said means for transmitting.

72. The system of Claim 71, further comprising a means for providing a reference clock signal to said means for transmitting and said means for receiving.

73. The system of Claim 71, wherein said means for receiving further comprises means for converting serial data to parallel data.

74. The system of Claim 73, wherein said means for transmitting further comprises means for converting parallel data from the means for receiving to serial data.

75. The system of Claim 71, further comprising (i) first means for communicating with one or more first external devices, communicatively coupled to said means for receiving and (ii) second port means for communicating with one or more second external devices, communicatively coupled to said means for transmitting.

76. A multiport device, comprising:

a) a plurality of means for receiving, each coupled to a unique one of a plurality of means for recovering a clock signal;

b) a plurality of means for transmitting serial data in accordance with a periodic signal, each of said plurality of means for transmitting being coupled to a unique one of a plurality of means for filtering recovered clock information from a

corresponding one of the plurality of means for recovering, and said periodic signal being adjusted in response to filtered recovered clock information; and

c) a plurality of means for transferring data from one of the plurality of means for receiving to one of the plurality of means for transmitting.

77. The multiport device of claim 76, further comprising a plurality of means for communicating with one or more external devices, a first subset of said plurality of means for communicating coupled to the plurality of means for receiving, and a second subset of said plurality of means for communicating coupled to said plurality of means for transmitting.

78. The multiport device of claim 76, further comprising a plurality of means for selecting from among said plurality of means for transferring data.

79. The multiport device of claim 78, wherein each of said plurality of means for selecting communicatively couple at least one of said first subset of said plurality of means for communicating to at least a subset of the plurality of means for receiving in the multiport device.

80. The multiport device of claim 78, wherein each of said plurality of means for selecting communicatively couple at least one of said second subset of said plurality of means for communicating to at least a subset of the plurality of means for transmitting in the multiport device.

81. The multiport device of claim 78, wherein each of said plurality of means for selecting communicatively couple at least a subset of the plurality of means for receiving to at least a subset of the plurality of means for transmitting in the multiport device.

82. A network, comprising:

a) a plurality of the systems of Claim 71; and

b) a plurality of means for data storing or data communications, each of said means for data storing or data communications being communicatively coupled to at least one of said systems.

83. The network of Claim 82, wherein said each of said plurality of said systems receives serial data from said plurality of means for data storing or data communications.

84. The network of Claim 82, wherein a first one of said plurality of means for data storing or data communications operates at a first frequency, a second one of said plurality of means for data storing or data communications operates at a second frequency the same as or different from the first frequency, and said plurality of said systems operates at a third frequency the same as or different from either or both of the first and/or second frequencies.

85. The network of Claim 84, wherein each of said first and second means for data storing or data communications and each of said plurality of said systems transmits serial data at a rate of at least 1 Gb/second.

86. The network of Claim 84, wherein each of said plurality of said systems transmits serial data at a rate F_3 that is about the same as at least one of a rate F_1 at which said first means for data storing or data communications transmits serial data and a rate F_2 at which said second means for data storing or data communications transmits serial data.

87. The network of Claim 82, further comprising a means for controlling a network.

88. The network of Claim 87, wherein said means for controlling said network comprises means for selecting a first one of said means for data storing or data communications from which serial data is to be transmitted, a second one of said means for data storing or data communications to which serial data is to be transmitted, and one of said systems to receive said serial data from said first means for data storing or data communications and transmit said serial data to said second means for data storing or data communications.

89. A method of facilitating data transfer, comprising the steps of:

a) determining a phase difference between a first periodic signal and a second periodic signal, said first periodic signal being recovered from a data stream;

b) adjusting said second periodic signal in response to said phase difference and filtered information from said first periodic signal; and

c) transmitting said data stream in accordance with said adjusted second periodic signal.

90. The method of Claim 89, further comprising receiving said data stream and recovering said first periodic signal therefrom.

91. The method of Claim 89, further comprising transferring data from said data stream to a transmitter configured to perform said transmitting step along a data path that does not include a first-in-first-out (FIFO) memory or an elastic buffer.

92. The method of Claim 89, further comprising filtering phase difference information corresponding to said phase difference.

93. The method of Claim 89, wherein said adjusting step comprises combining said filtered phase difference information with said filtered information from said first periodic signal.

94. The method of Claim 89, further comprising the step of filtering said information from said first periodic signal.

95. The method of Claim 94, wherein said information from said first periodic signal comprises recovered clock adjustment information.

96. The method of Claim 95, wherein said recovered clock adjustment information is configured to adjust a phase and/or frequency of said first periodic signal.

97. The method of Claim 96, wherein said recovered clock adjustment information is configured to adjust a phase of said first periodic signal.

98. The method of Claim 89, wherein the step of filtering said information further comprises tracking a frequency of said first periodic signal.